DATA SHEET

TDA8772

Triple 8-bit video digital-to-analog converter

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Triple 8-bit video digital-to-analog converter	TDA8772

FEATURES

- 8-bit resolution
- Sampling rate up to:
  - 35 MHz for TDA8772H/3
  - 85 MHz for TDA8772H/8
- Internal reference voltage regulator
- No deglitching circuit required
- $\overline{SYNC}$, $\overline{BLANK}$ control inputs
- 3 independent clock inputs (one per DAC)
- 1 V output voltage range
- 75 Ω output load
- TDA8772 has $\overline{BLANK}$ control on the 3 channels
- Single 5 V power supply
- 44-pin QFP package.

APPLICATIONS

- General purpose high-speed digital-to-analog conversion
- Digital TV
- Graphic display
- Desktop video processing.

GENERAL DESCRIPTION

The TDA8772 is a triple 8-bit video Digital-to-Analog Converter (DAC). It converts the digital input signals into analog voltage outputs at a maximum conversion rate of 35 MHz (TDA8772H/3) and 85 MHz (TDA8772H/8).

The DAC is based on resistor-string architecture with integrated output buffers. The output voltage range is determined by a built-in reference source.

The device is fabricated in a 5 V CMOS process that ensures high functionality with low power dissipation.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			SAMPLING FREQUENCY
	NAME	DESCRIPTION	VERSION	
TDA8772H/3	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2	35 MHz
TDA8772H/8				85 MHz

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QUICK REFERENCE DATA

| SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	$R_L = 75\ \Omega$; note 1	40	65	100	mA
I_{DDD}	digital supply current					
	TDA8772H/3		–	7	16	mA
	TDA8772H/8		–	16	27	mA
INL	integral non-linearity2	$f_{clk} = 35$ MHz; ramp input	–	±0.5	±1	LSB
		$f_{clk} = 85$ MHz; ramp input	–	±0.75	±1.2	LSB
DNL	differential non-linearity	$f_{clk} = 35$ MHz; ramp input	–	±0.25	±0.5	LSB
		$f_{clk} = 85$ MHz; ramp input	-	±0.5	±0.75	LSB
$f_{clk(max)}$	maximum clock frequency					
	TDA8772H/3		35	–	–	MHz
	TDA8772H/8		85	–	–	MHz
P_{tot}	total power dissipation	note 1				
	TDA8772H/3	$R_L = 75\ \Omega$; $f_{clk} = 35$ MHz	180	360	640	mW
	TDA8772H/8	$R_L = 75\ \Omega$; $f_{clk} = 85$ MHz	180	405	700	mW

Note

1. Minimum and maximum data of current and power consumption are measured in worse case conditions: for minimum data, all digital inputs are at logic level 0 while for maximum data, all digital inputs are at logic level 1.

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BLOCK DIAGRAM

Fig.1 Block diagram.

MBB661 - 2
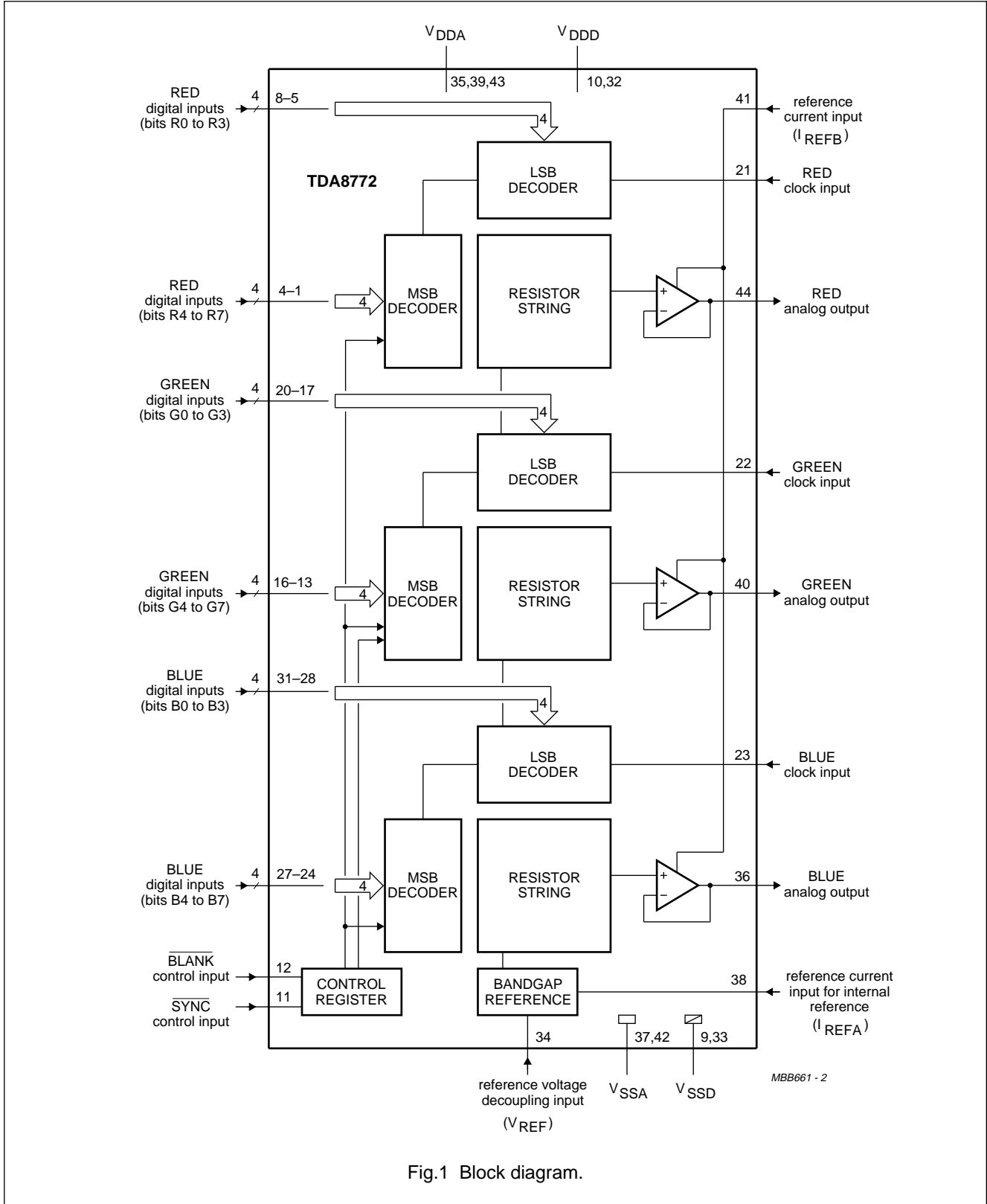
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PINNING

SYMBOL	PIN	DESCRIPTION
R7	1	RED digital input data; bit 7 (MSB)
R6	2	RED digital input data; bit 6
R5	3	RED digital input data; bit 5
R4	4	RED digital input data; bit 4
R3	5	RED digital input data; bit 3
R2	6	RED digital input data; bit 2
R1	7	RED digital input data; bit 1
R0	8	RED digital input data; bit 0 (LSB)
V_{SSD1}	9	digital supply ground 1
V_{DDD1}	10	digital supply voltage 1
$\overline{SYNC}$	11	composite sync control input; for GREEN channel only (active LOW)
$\overline{BLANK}$	12	composite blank control input (active LOW)
G7	13	GREEN digital input data; bit 7 (MSB)
G6	14	GREEN digital input data; bit 6
G5	15	GREEN digital input data; bit 5
G4	16	GREEN digital input data; bit 4
G3	17	GREEN digital input data; bit 3
G2	18	GREEN digital input data; bit 2
G1	19	GREEN digital input data; bit 1
G0	20	GREEN digital input data; bit 0 (LSB)
CLKR	21	RED clock input
CLKG	22	GREEN clock input

SYMBOL	PIN	DESCRIPTION
CLKB	23	BLUE clock input
B7	24	BLUE digital input data; bit 7 (MSB)
B6	25	BLUE digital input data; bit 6
B5	26	BLUE digital input data; bit 5
B4	27	BLUE digital input data; bit 4
B3	28	BLUE digital input data; bit 3
B2	29	BLUE digital input data; bit 2
B1	30	BLUE digital input data; bit 1
B0	31	BLUE digital input data; bit 0 (LSB)
V_{DDD2}	32	digital supply voltage 2
V_{SSD2}	33	digital supply ground 2
V_{REF}	34	decoupling input for reference voltage
V_{DDA1}	35	analog supply voltage 1
OUTB	36	BLUE analog output
V_{SSA1}	37	analog supply ground 1
I_{REFA}	38	reference current input for internal reference
V_{DDA2}	39	analog supply voltage 2
OUTG	40	GREEN analog output
I_{REFB}	41	reference current input for output buffers
V_{SSA2}	42	analog supply ground 2
V_{DDA3}	43	analog supply voltage 3
OUTR	44	RED analog output

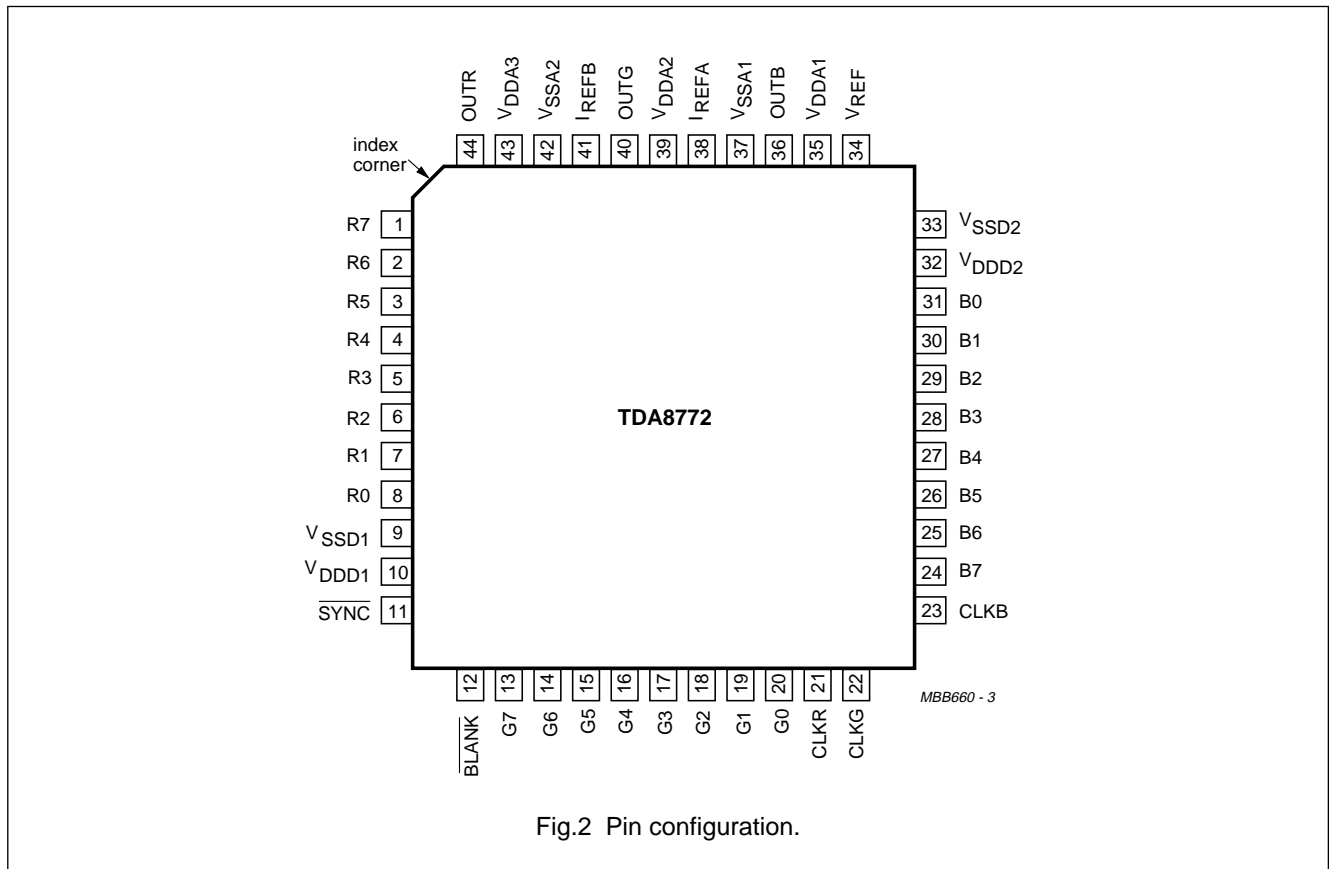## Triple 8-bit video digital-to-analog converter

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Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	−0.5	+6.5	V
V_{DDD}	digital supply voltage	−0.5	+6.5	V
ΔV_{DD}	supply voltage difference between V_{DDA} and V_{DDD}	−1.0	+1.0	V
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	0	70	°C
T_j	junction temperature	−	125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

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CHARACTERISTICS

TDA8772H/3 operating at 35 MHz and TDA8772H/8 operating at 85 MHz unless otherwise specified.

$V_{DDA} = V_{DDD} = 4.5$ V to 5.5 V; V_{SSA} and V_{SSD} shorted together; $V_{DDA} - V_{DDD} = -0.5$ V to +0.5 V; $T_{amb} = 0$ to +70 °C; typical values measured at $V_{DDA} = V_{DDD} = 5$ V and $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	$R_L = 75$ Ω; note 1	40	65	100	mA
I_{DDD}	digital supply current					
	TDA8772H/3		–	7	16	mA
	TDA8772H/8		–	16	27	mA
Inputs						
CLOCK INPUTS (PINS 21 TO 23)						
V_{IL}	LOW level input voltage		$V_{SSD} - 0.5$	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	$V_{DDD} + 0.5$	V
BLANK, SYNC INPUTS (PINS 12 AND 11; ACTIVE LOW)						
V_{IL}	LOW level input voltage		$V_{SSD} - 0.5$	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	$V_{DDD} + 0.5$	V
R, G, B DIGITAL INPUTS (PINS 1 TO 8, 13 TO 20 AND 24 TO 31)						
V_{IL}	LOW level input voltage		$V_{SSD} - 0.5$	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	$V_{DDD} + 0.5$	V
I_{REFA} INTERNAL REFERENCE SUPPLY CURRENT (PIN 38)						
$I_{i(REFA)}$	input current		–	0.17	0.25	mA
I_{REFB} OUTPUT BUFFER SUPPLY CURRENT (PIN 41)						
$I_{i(REFB)}$	input current		–	0.5	0.7	mA
Timing ($C_L = 25$ pF; $R_L = 75$ Ω); see Fig.3						
$f_{clk(max)}$	maximum clock frequency					
	TDA8772H/3		35	–	–	MHz
	TDA8772H/8		85	–	–	MHz
t_{CPH}	clock pulse width HIGH		5	–	–	ns
t_{CPL}	clock pulse width LOW		5	–	–	ns
t_r	clock rise time					
	TDA8772H/3		–	–	5	ns
	TDA8772H/8		–	–	3	ns
t_f	clock fall time					
	TDA8772H/3		–	–	5	ns
	TDA8772H/8		–	–	3	ns
$t_{SU;DAT}$	input data set-up time		4	–	–	ns
$t_{HD;DAT}$	input data hold time		2.5	–	–	ns

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage reference (pin 34, referenced to V_{SSA})						
V_{ref}	output reference voltage		1.180	1.242	1.305	V
Outputs						
OUTB, OUTR, OUTG ANALOG OUTPUTS (PINS 36, 44 AND 40, REFERENCED TO V_{SSA}) R_L = 75 Ω; SEE TABLES 1 AND 2						
FSR	full-scale output voltage range		0.9	1.0	1.1	V
V_{os}	offset of analog voltage output		0.75	0.83	0.95	V
V_{OUTmax}	maximum output voltage	data inputs = logic 1; note 2	1.65	1.83	2.05	V
V_{OUTmin}	minimum output voltage	data inputs = logic 0; note 2	0.75	0.83	0.95	V
THD	total harmonic distortion	f_i = 4.43 MHz; f_{clk} = 35 MHz	–	–45	–	dB
		f_i = 4.43 MHz; f_{clk} = 85 MHz	–	–43	–	dB
Z_L	output load impedance		60	75	90	Ω
Transfer function						
INL	integral non-linearity	f_{clk} = 35 MHz; ramp input	–	$\pm$0.5	$\pm$1	LSB
		f_{clk} = 85 MHz; ramp input	–	$\pm$0.75	$\pm$1.2	LSB
DNL	differential non-linearity	f_{clk} = 35 MHz; ramp input	–	$\pm$0.25	$\pm$0.5	LSB
		f_{clk} = 85 MHz; ramp input	-	$\pm$0.5	$\pm$0.75	LSB
α_{CT}	crosstalk DAC to DAC		–45	–	–	dB
m	DAC to DAC matching		–	1.0	2.0	%
Switching characteristics (R_L = 75 Ω); see Fig.4						
t_d	input to 50% output delay time	full-scale change	–	10	–	ns
t_{s1}	settling time	10% to 90% full-scale change	–	6	–	ns
t_{s2}	settling time	to $\pm$1 LSB	–	30	–	ns
Output transients (glitches)						
V_g	area for 1 LSB change		–	1	–	LSB.ns

Notes

1. Minimum and maximum data of current and power consumption are measured in worse case conditions: for minimum data, all digital inputs are at logic level 0 while for maximum data, all digital inputs are at logic level 1.

2. V_{OUT} is directly proportional to V_{ref}.

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Table 1   Input coding and DAC output voltages (typical values)

BINARY INPUT DATA (SYNC = BLANK = 0)	CODE	DAC OUTPUT VOLTAGES (V) OUTB, OUTR, OUTG $R_L = 75\ \Omega$
0000 0000	0	0.830
0000 0001	1	0.834
....	.	.
1000 0000	128	1.330
....	.	.
1111 1110	254	1.826
1111 1111	255	1.830

Table 2   Input coding and DAC output voltages (typical values)

BINARY INPUT DATA	$\overline{\text{SYNC}}$ (PIN 11)	$\overline{\text{BLANK}}$ (PIN 12)	DAC OUTPUT VOLTAGES (V)	
			OUTG (PIN 40)	OUTR/B (PINS 44, 46)
....	x	1	see Table 1	see Table 1
....	1	0	0.830	0.830
....	0	0	0.440	

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TIMING
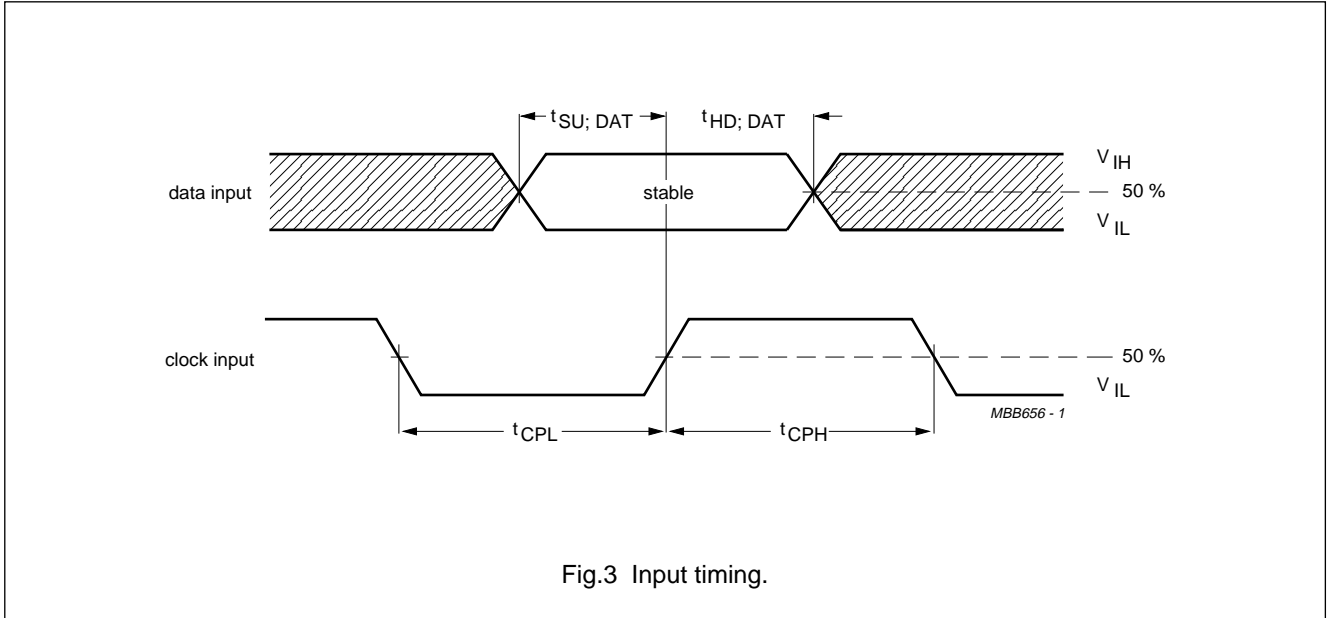
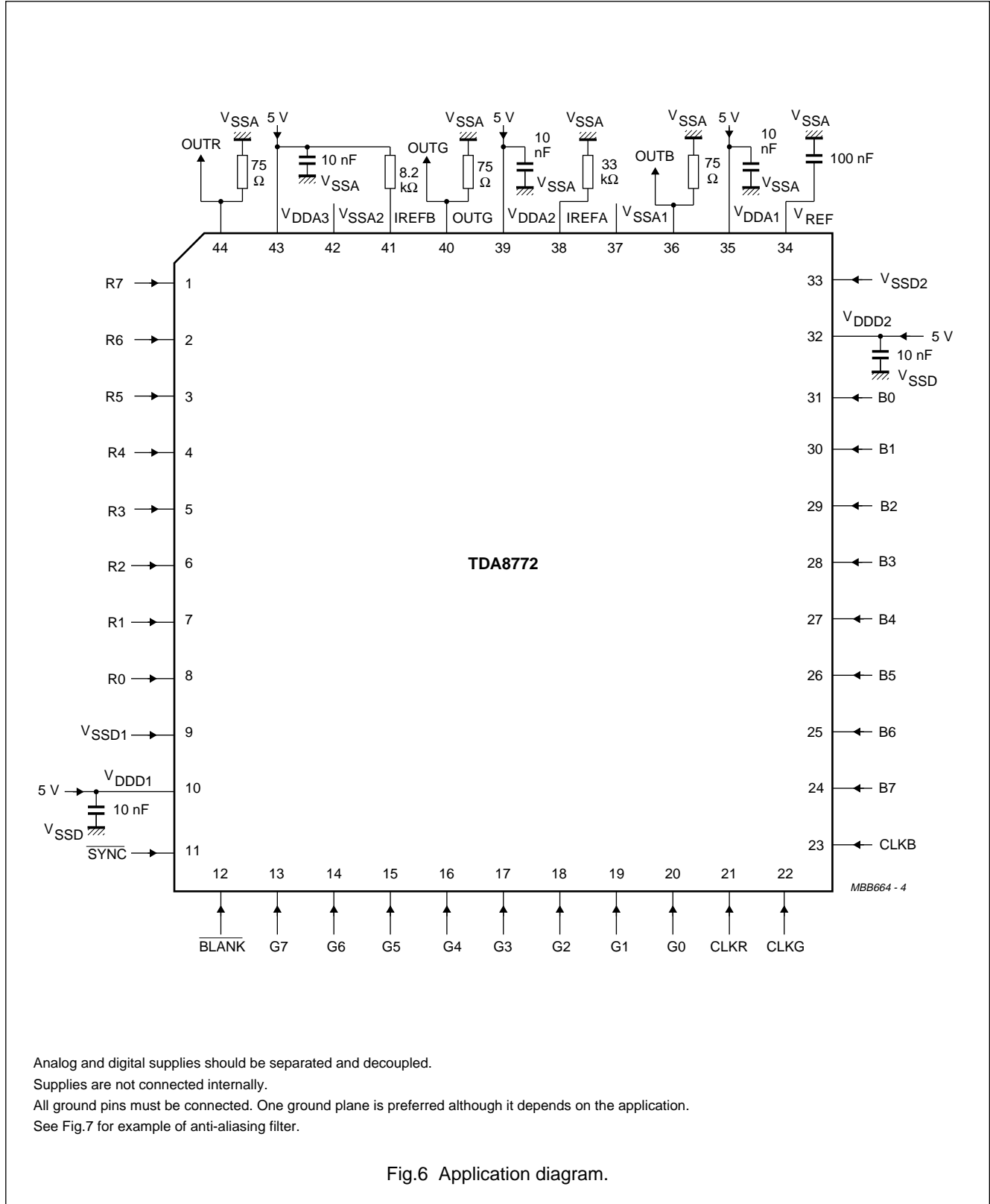Fig.3 Input timing.
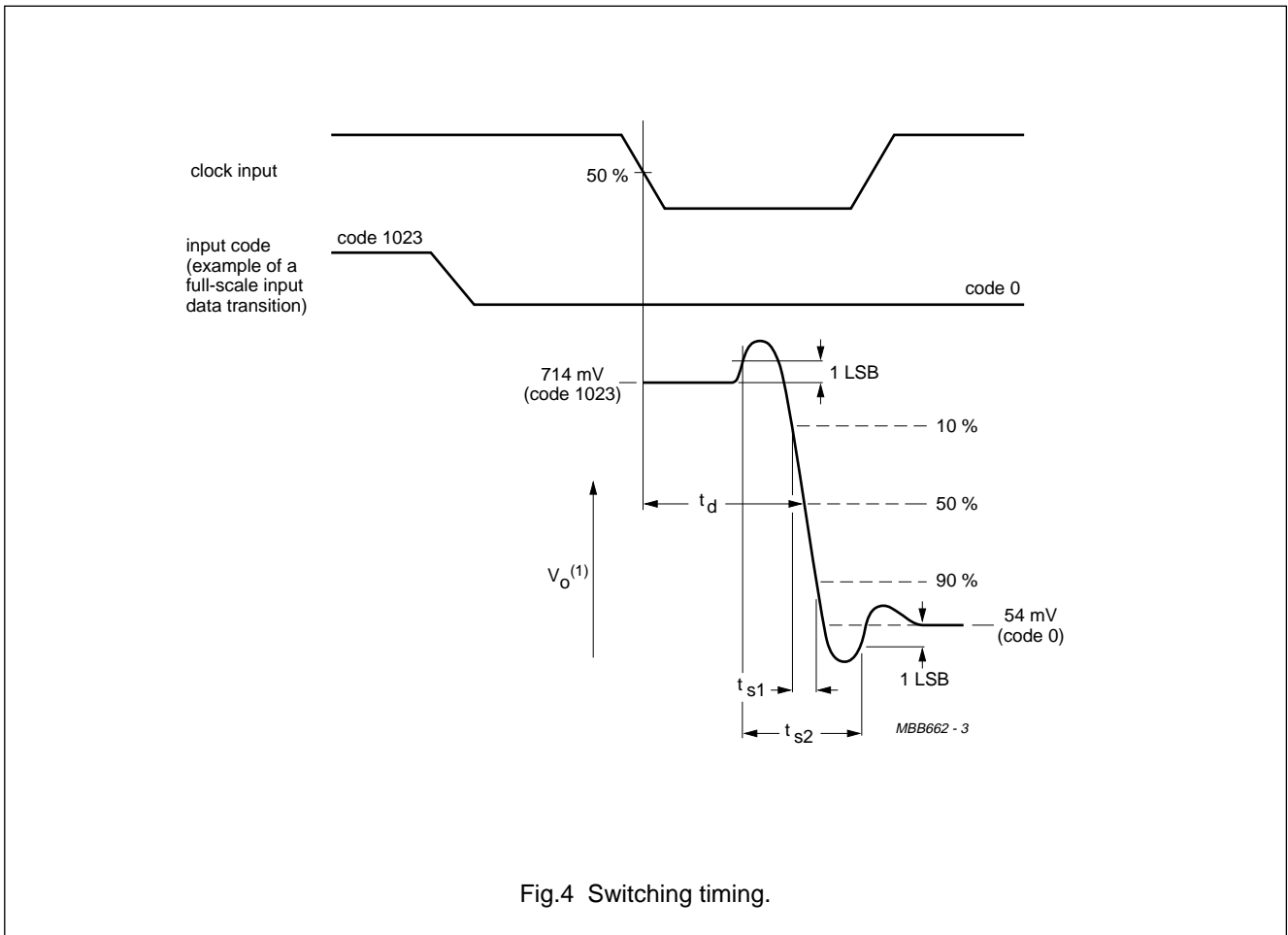
Fig.4 Switching timing.
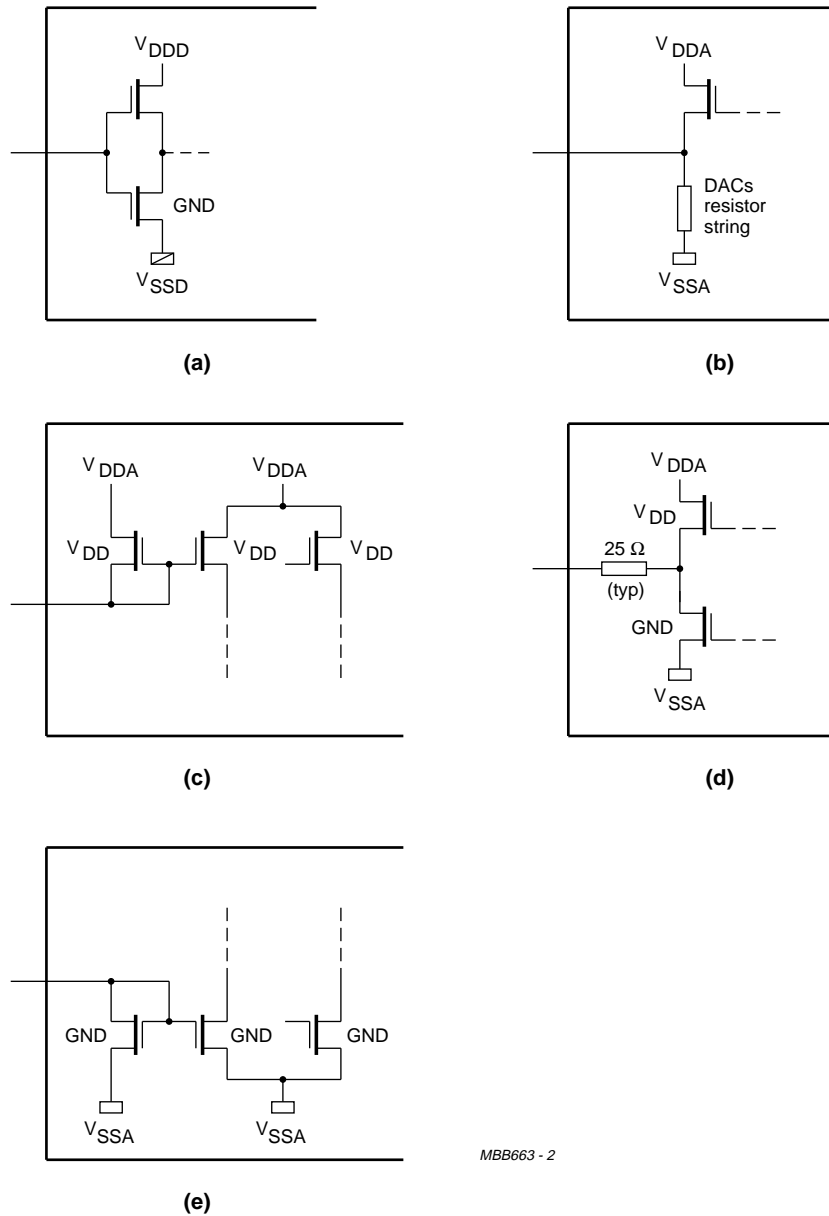
INTERNAL CIRCUITRY

(a) Digital inputs; pins 1 to 8 and 11 to 31.

(b) V_{ref}; pin 34.

(c) I_{REFA}; pin 38.

(d) OUTR, G, B; pins 44, 40 and 36.

(e) I_{REFB}; pin 41.

Fig.5 Internal circuitry.

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APPLICATION INFORMATION

Analog and digital supplies should be separated and decoupled.

Supplies are not connected internally.

All ground pins must be connected. One ground plane is preferred although it depends on the application.

See Fig.7 for example of anti-aliasing filter.

Fig.6 Application diagram.
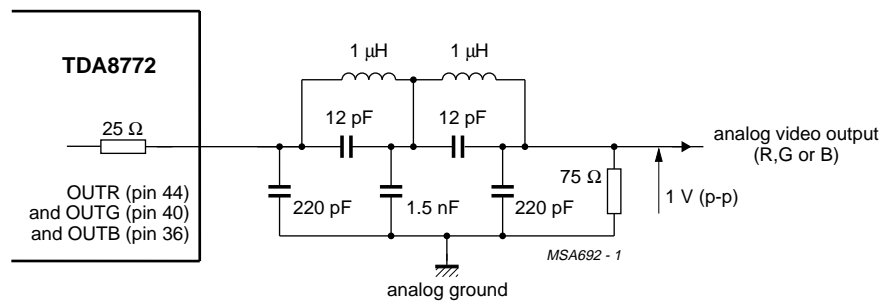
Fig.7 Example of anti-aliasing filter for 1 V output swing.
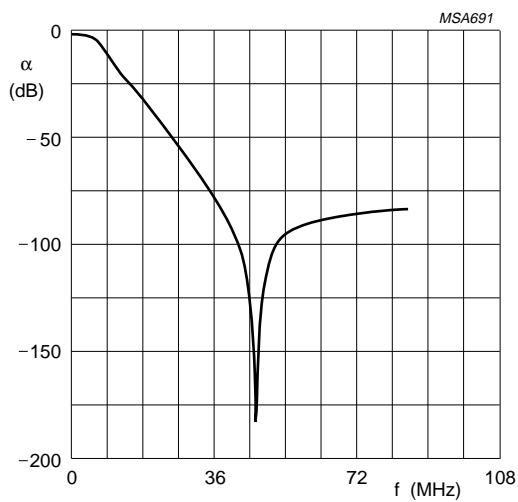
Fig.8 Frequency response for filter shown in Fig.7.

Characteristics of Fig.8

• Order 5; adapted CHEBYSHEV

• Ripple $\rho \geq 0.6$ dB

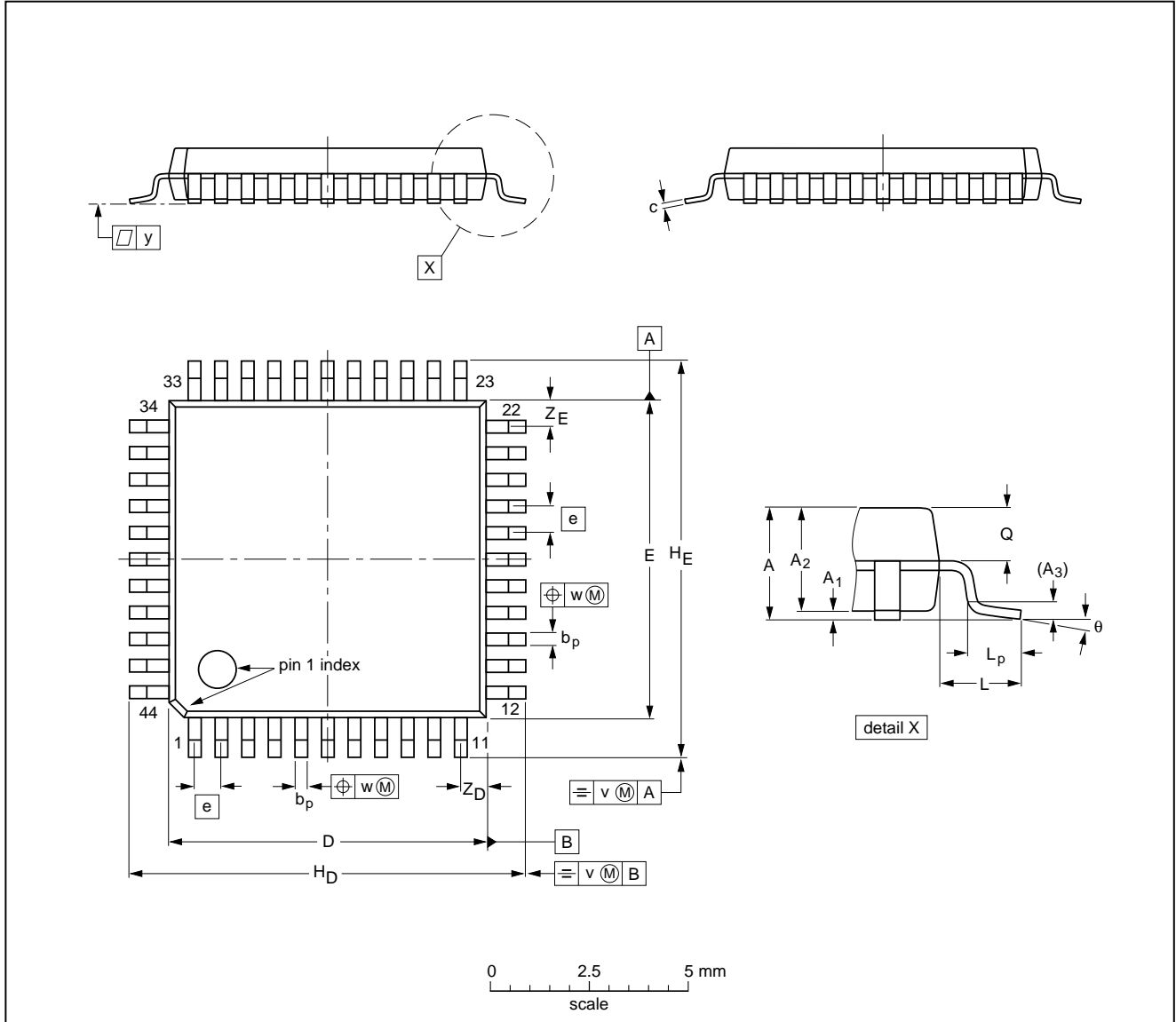• Frequency at -3 dB = 6.5 MHz

• f_{NOTCH} = 46 MHz.

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PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**

detail X

0   2.5   5 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						92-11-17 95-02-04

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**

- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580/xxx

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,
Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2870, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

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Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

Printed in The Netherlands   547047/1200/06/pp20   Date of release: 1997 Mar 06   Document order number: 9397 750 01836

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